MicroTCA at FNAL

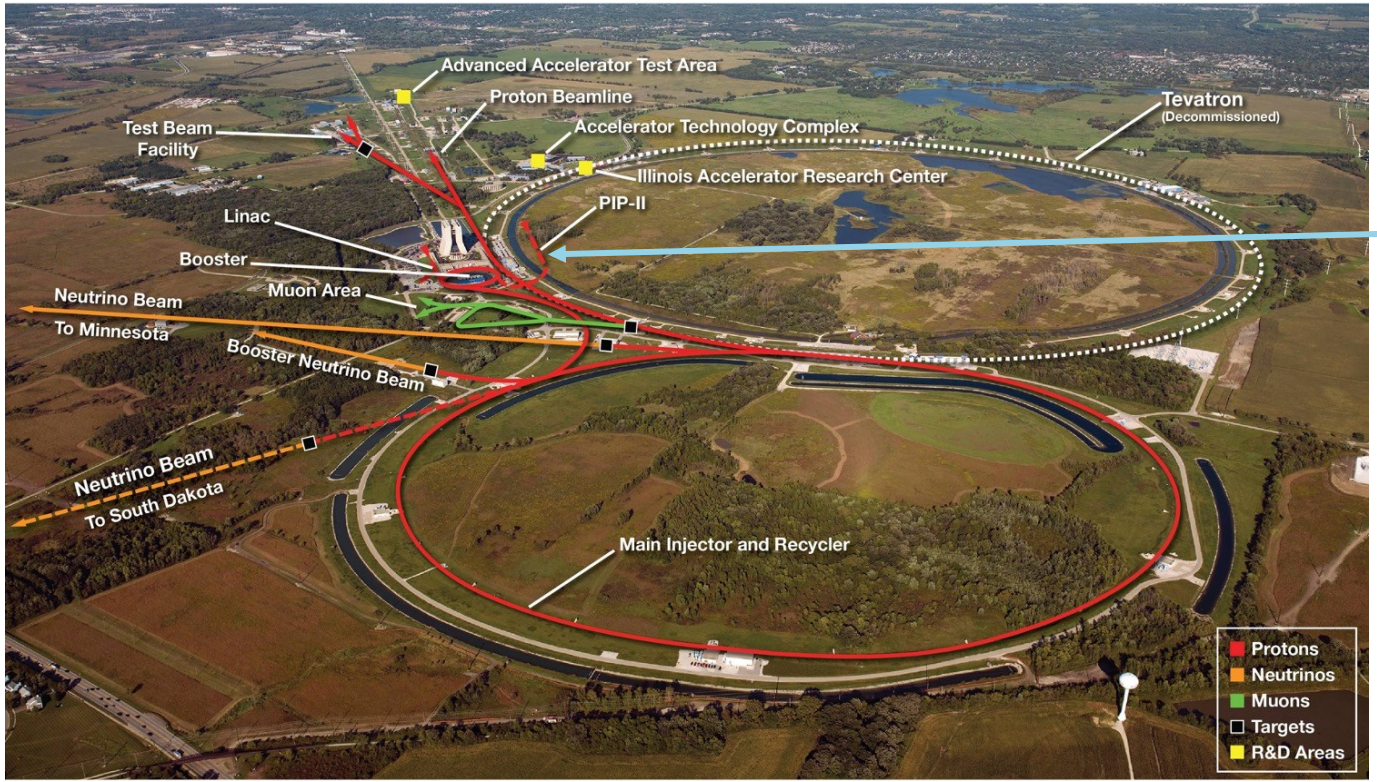
Jennifer Case
µTCA Working Group, EPICS Collaboration Meeting
16 September 2024

This work was produced by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11359 with the U.S. Department of Energy, Office of Science, Office of High Energy Physics.

Overview

- Overview of Fermilab
- MicroTCA and Instrumentation
- MicroTCA and Controls for the ACORN Project

Overview of Fermilab

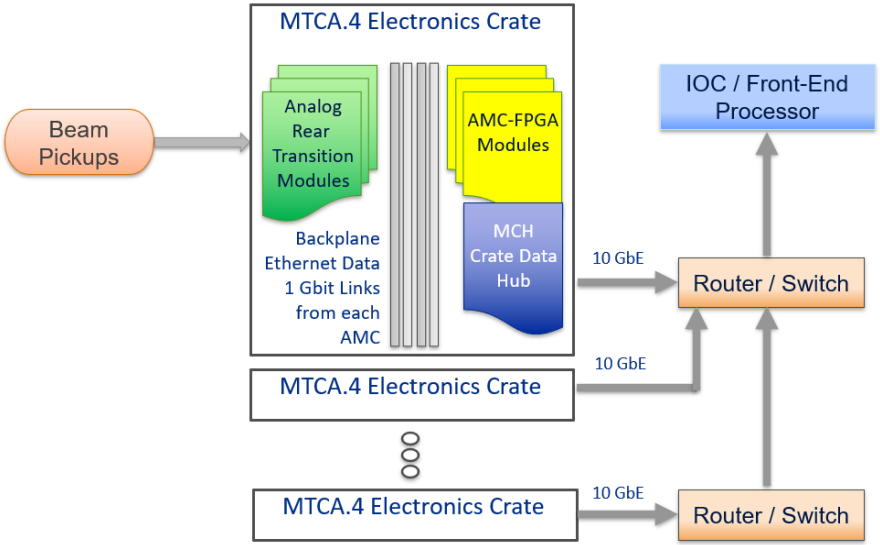


MicroTCA and Instrumentation

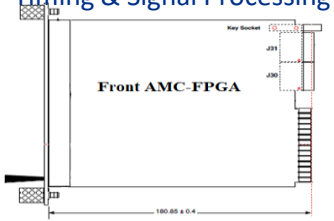
Instrumentation MicroTCA

- MicroTCA was chosen as the new platform for Instrumentation systems
  - Beam Position Monitors (BPMs), Beam Loss Monitors (BLMs), Beam Current Monitors (BCMs), etc.
- Ethernet was chosen as the primary transport utilizing a streaming service (Redis) to interact with EPICS soft IOCs in rack mount servers
  - Utilizing Fabric A only via 1G ethernet and using the MCH as an aggregation switch (10G-40G)
- PIP-II
  - PIP-II: 20 crates with ~150 AMCs
  - MI8 BPM: 6 crates with ~30 AMCs
- Working primarily with Vadatech to develop AMCs to our requirements
- Vetting other suppliers for hardware components (power supplies, crates, MCH)

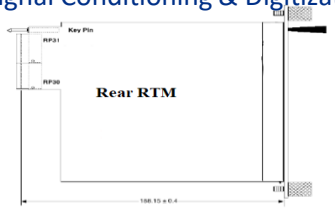
MicroTCA, MTCA.4 DAQ Platform



Timing & Signal Processing



Signal Conditioning & Digitization



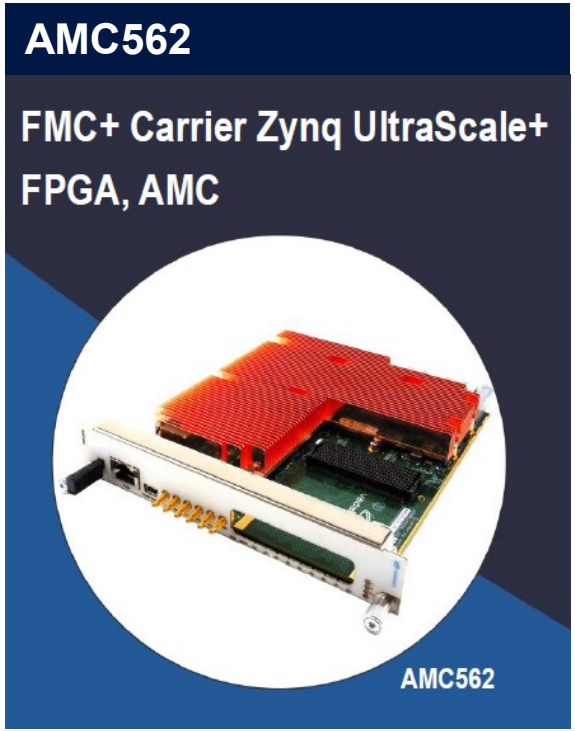
The AMC-FPGA module and RTM module will comply with the following MTCA standards

- PICMG® AMC.0 R2.0 Advanced Mezzanine Card Base Specification
- PICMG® AMC.2 Revision 1.0 Ethernet Advanced Mezzanine Card Specification
- PICMG® MTCA.0 R2.0 Micro Telecommunications Computing Architecture Base Specification
- PICMG® MTCA.4 R 1.0 MicroTCA Enhancements for Rear I/O and Precision Timing

Fermilab

MicroTCA AMC and RTM

- Choice was made to contract a vendor to build AMC FPGA modules to our needs.
  - We wanted to build off the vendors knowledge of MicroTCA.
  - We benefit from more quality controls and documentation.
  - We have a product we can buy for upcoming accelerator improvement projects.
- Detailed requirements for two types of AMCs were written and put out for bid.
  - Goals were to have products that meet our needs at the best price.
  - One AMC for lower sample rate applications (<125 Msps).
  - One AMC for higher sample rate applications (>125 Msps).
  - The first AMC received bids from two vendors.
- Choice was made to continue to design the RTMs in-house.
  - We have several applications that require custom circuits
  - We want to build and maintain in house design talent to support our complex.



Xilinx UltraScale+ XCZU7EV FPGA

Double module, mid-size

FMC+ site (All LA and HA LVDS, 16 Gigabit XCVRs)

8 GB of 64-bit wide DDR4 Memory (single bank) with ECC PS, ARM processor side only.

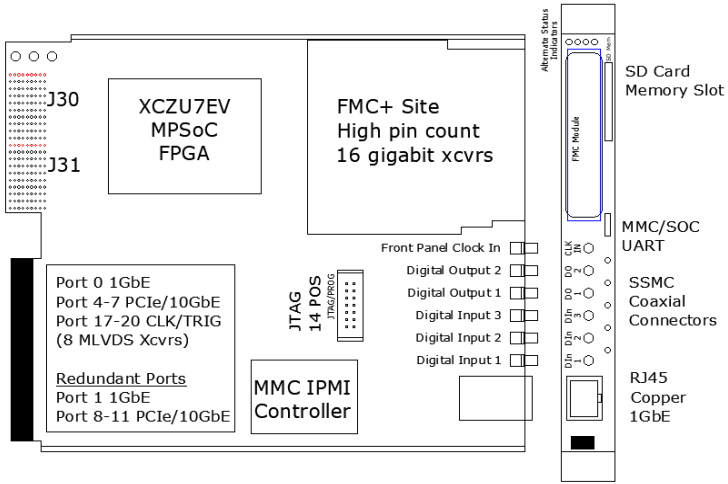
SD Card (option)

128 MB of Boot Flash

64 GB of User Flash

Clock Jitter Cleaner

Zone 3 -- DESY Class D1.0
48 LVDS IO



Used with BLMs and BCMs and lower digitizer sample rate applications.

~$3,000.00 each

Fermilab

Xilinx UltraScale+ XCZU7EV FPGA

Double module, mid-size

FMC+ site (All LA and HA LVDS, 4 Gigabit XCVRs)

8 GByte of 64-bit wide DDR4 Memory (single bank) with ECC PS, ARM processor side.

8 GByte of 64-bit wide DDR4 Memory (single bank) with ECC PL, FPGA fabric side.

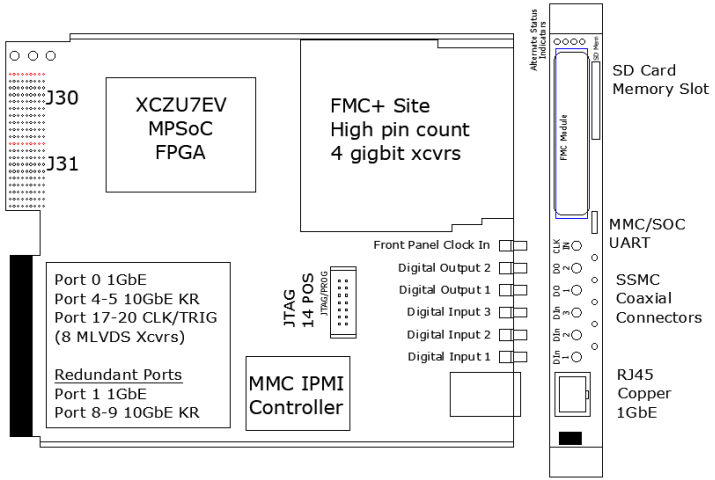
SD Card (option)

128 MB of Boot Flash

64 GB of User Flash

Clock Jitter Cleaner

Zone 3 - DESY D1.4 Specification
~16 LVDS IO
16 high speed Receivers
16 high speed Transmitters



Used with BPMs and higher digitizer sample rate applications.

~$6,000.00 each

Fermilab

MicroTCA.4 RTM for the AMC566

DESY D1.4 Specification

4x TI ADS42JB69

Total of 8 ADC 16-bit @ 250MSPS

Clock input for synchronization

~$4,000.00 each

This module currently does not have all the signal conditioning circuits we need for the BPM application.

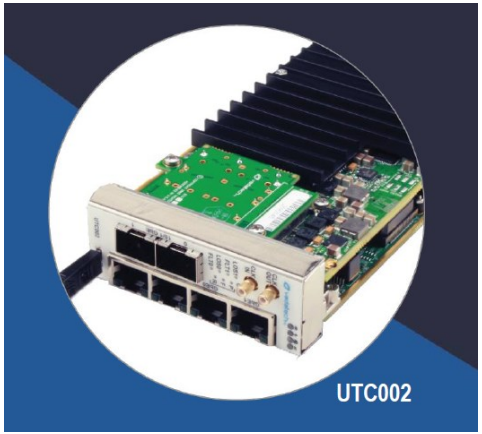
The module was included with the development of the AMC566 so the JESD204B links and firmware could be developed and verified at the vendor.

MicroTCA Controller Hub (MCH)

We are evaluating MCHs from both Vadatech and N.A.T.

Our requirements are simple:

- 1 GbE, Port 0 links to 12 AMCs
- Aggregated uplink out the front at 10 GbE or greater.

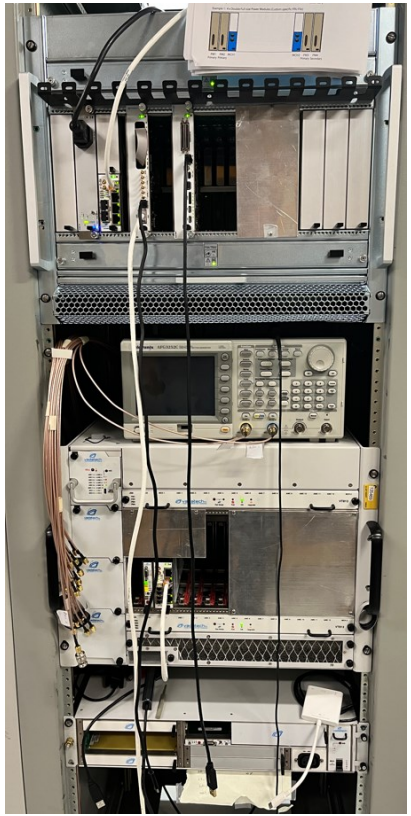


Fermilab

MTCA.4 Chassis, Power Modules, and Cooling units

The components are being evaluated from three vendors.

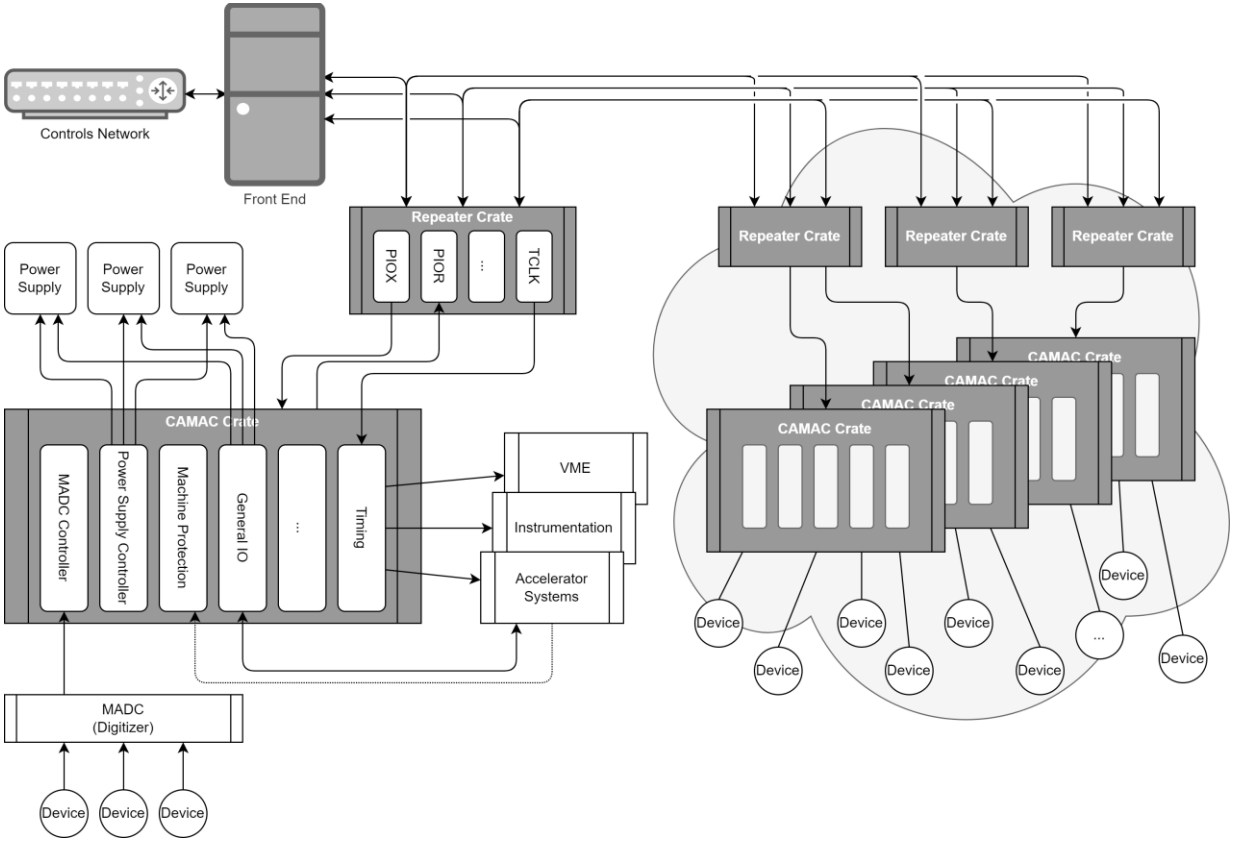
Vadatech, Inc.
NVent-Schroff
N.A.T.



Fermilab

MicroTCA and Controls for the ACORN Project

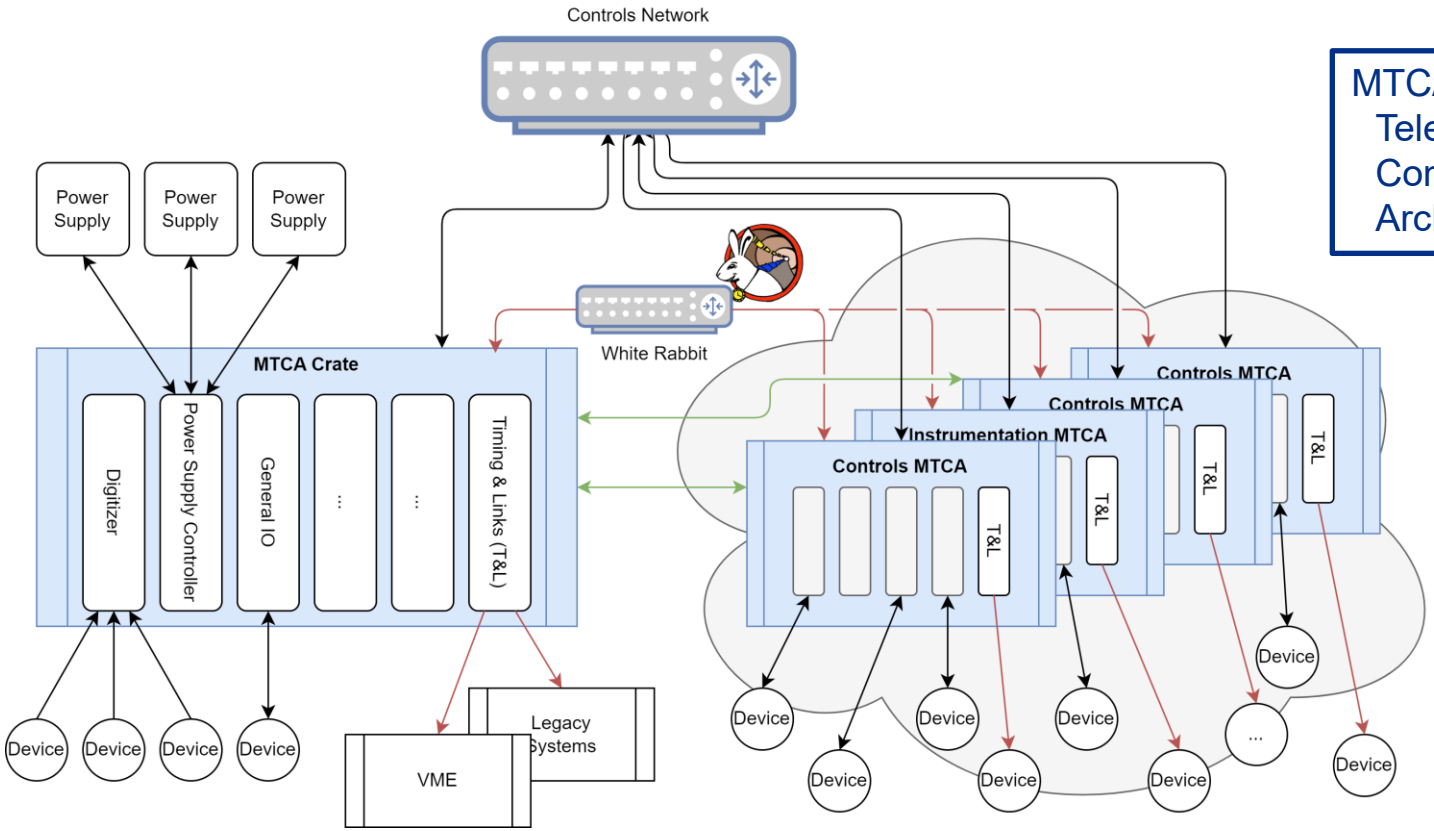
Current CAMAC-based Controls Hardware



PIOX – CAMAC Link
PIOR – CAMAC Link
TCLK – Real-time Event-based Clock
MADC – Multiplexed Analog-to-Digital Converter

Fermilab

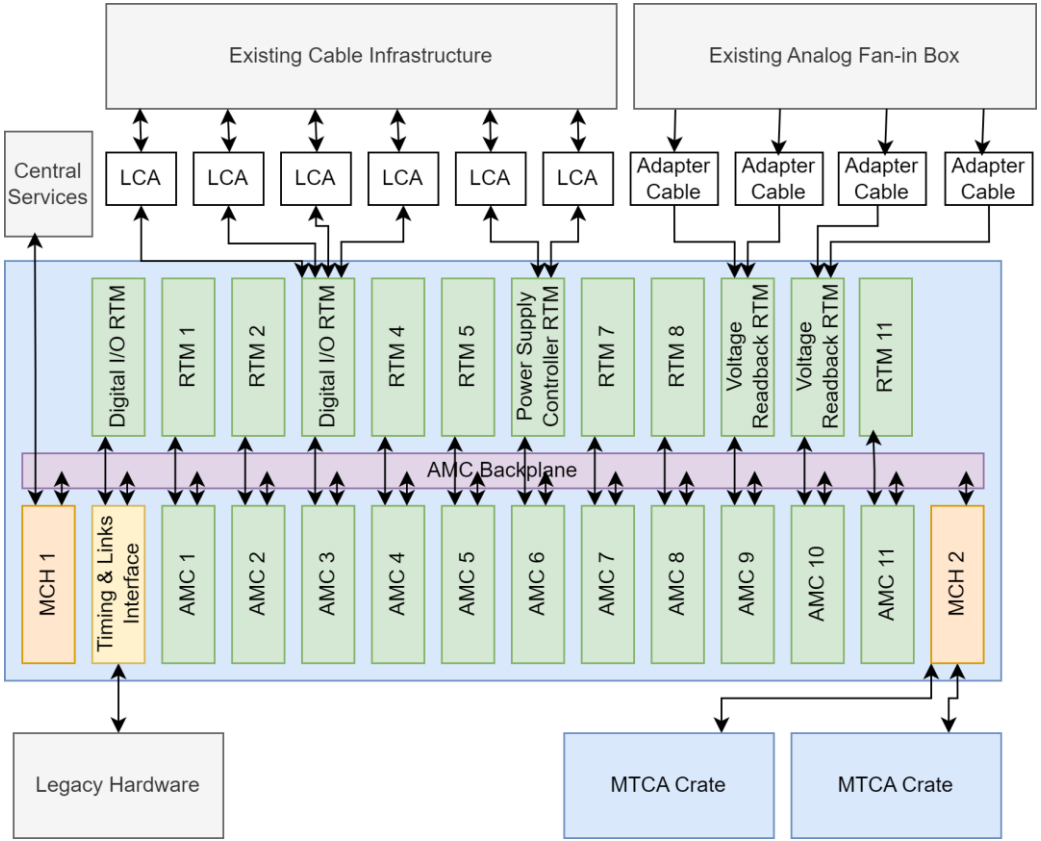
MicroTCA-based Conceptual Design



MTCA – Micro Telecommunications Computing Architecture

Fermilab

MicroTCA-based Conceptual Design

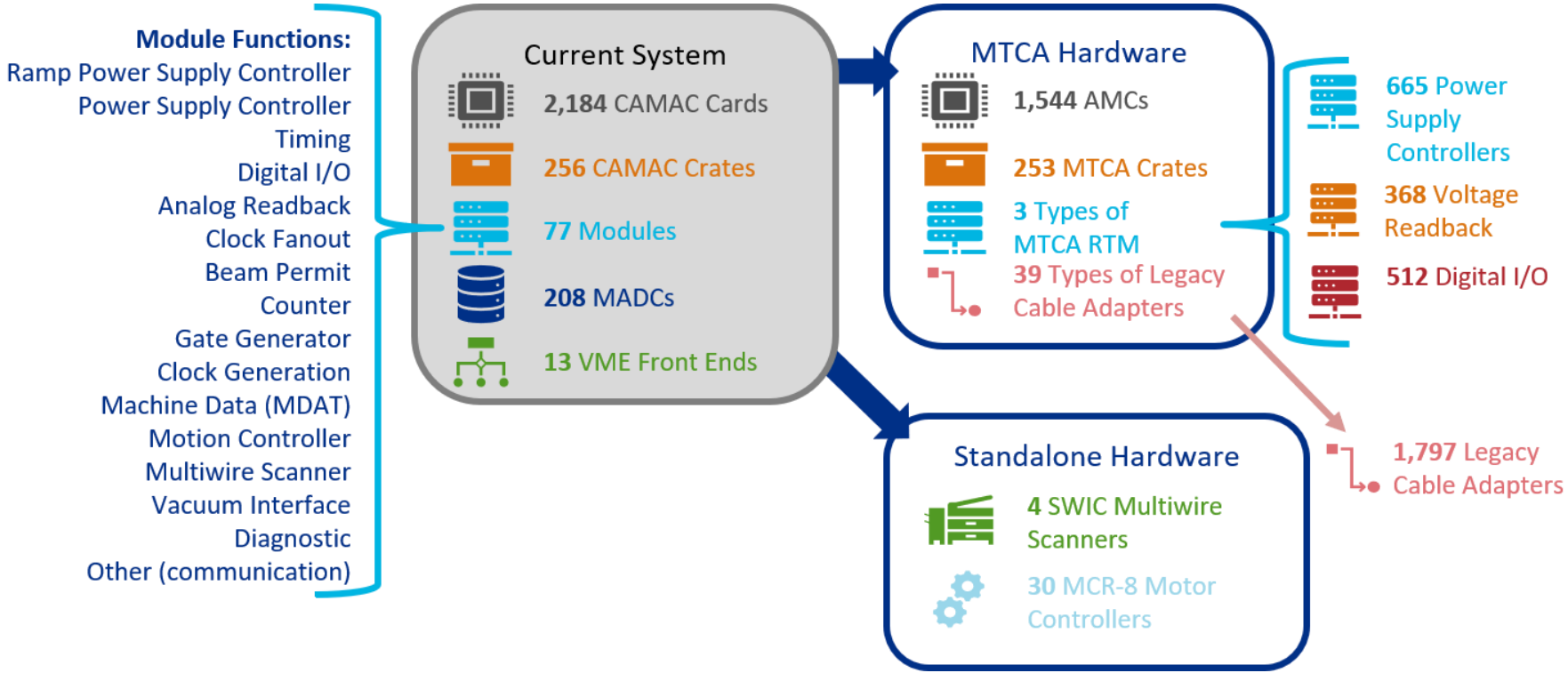


AMC – Advanced Mezzanine Card
LCA – Legacy Cable Adapter
MCH – MTCA Carrier Hub
RTM – Rear Transition Module

AMCs – Commercial Off-the-Shelf
RTMs – Designed In-house

Fermilab

Summary of ACORN Hardware



Fermilab

Summary

- Fermilab is replacing its existing hardware solutions that use obsolete or near-obsolete standards with a modern hardware solution (MicroTCA)
  - Instrumentation is moving to MicroTCA as their hardware solution
  - The ACORN Project is planning to use MicroTCA for Controls
  - The ACORN Project plans to utilize engineers across the lab to design hardware, spreading knowledge of MicroTCA throughout the lab